AMENDMENTS TO THE SPECIFICATION

IN THE SPECIFICATION:

Please replace the paragraph beginning on page 19, line 5 with the following rewritten paragraph.

$$V_2 = \Phi_0 + 1/3 * V_S + \delta V \qquad (10)$$

Please replace the paragraph beginning on page 22, line 4 with the following rewritten paragraph.

With reference to fig. 9 a discussion of a ferroelectric memory device adapted for implementing the method according to the invention shall be given. Some of its component parts have already been discussed in connection with fig. 3 and shall hence only be briefly mentioned. As before the memory matrix 300 comprises memory cells 420 between or at a crossings of word lines WL and bit lines BL in the matrix. The matrix is shown as an m·n matrix, i.e. with m word lines WL and n bit lines BL. The bit lines BL are connected to a sense amplifier bank 306, comprising a plurality of sense amplifiers SA and each connected with a bit line BL, thus allowing a full row read. However, in order to reduce the number of sense amplifiers the word lines may be segmented such that each segment comprises a certain number n/k of bit lines BL, where k is an integer, and correspondingly the sense amplifier bank 306 then shall

comprise n/k sense amplifiers. This implies that a multiplexer 905 must be provided for connecting each bit line on an addressed segment to one of the sense amplifiers SA for enabling a parallel read or write to all memory cells in a word line segment as is the case. In other words, the multiplexer 905 shall not be provided in case the memory device supports a full row addressing, i.e. to all memory cells on a word line in parallel. The driver circuits viz. the x driver 901 and the y driver 902 may replace the charge pump mechanism 340 in fig. 3, but are generally provided for applying the voltage pulses according to the given voltage pulse protocol to respectively the word lines WL and the bit lines BL. The selection of memory cells 420 for e.g. read or write operations takes place directly in the addressing operation via the x decoder 32 and the y decoder 302, whereby preferably word lines WL and bit lines BL may be selected as active by respectively a pull-up or pull-down from the same permanent quiescent voltage level chosen as a fraction of switching voltage V_S referred to zero (or floating ground), while inactive word lines and bit lines remain on quiescent potential or are pulled to another fractional voltage referred to V_S. On bit lines BL_{ref1} and BL_{ref2} there are shown respectively two reference memory cells 420A and 420B which may be set to respectively the first and the second polarization state, i.e. in other words represent a logical 0 and a logical 1. The reference cells 420A and 420B are respectively connected

with bit lines BL_{ref1} and BL_{ref2} and form a part of the memory matrix in the same manner as the other memory cells 420 and hence will be subjected to same disturbing influences or dynamic changes that may occur in the other memory cells, whether due to addressing operations, environmental factors and so on. – It should be understood that a pair of reference cells may be provided on every word line WL in a similar manner. – The reference memory cells 420A and 420B are addressed in a read operation and the result is detected via the sense amplifier bank 306 and output to the unit 900 for determining a switching speed. Consequently unit 900 has a clock input CLK. The switching speed is output to the calibration memory 702 which has an output connected with a pulse length controller 903, while as before another output is connected to the pulse amplitude controller 904, both controllers 903, 904 of course being connected to the memory control logic or unit 320. The memory device in addition may comprise a temperature sensor ~~702~~ 706 for sensing a working temperature of the memory and likewise of course with its output connected to the calibration memory 702.

Please replace the paragraph beginning on page 23, line 15 with the following rewritten paragraph.

As an optional feature a signal analyser 906 with clock input CLK is shown connected with output from the reference memory cells 420A, 420B. It can be used for carrying out a more sophisticated analysis, not only of the switching speed characteristics, but e.g. also in regard of polarization response characteristics of the memory cells. The output of the signal analyser 906 is connected with the calibration memory 702.